DESIGN OF PULSE TRIGGERED FLIPFLOP IN 90NM TECHNOLOGY FOR IMPROVED PERFORMANCE

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Abstract - The low power dissipation is the main goal of VLSI circuit designs. The reduction of power consumption in flipflop leads to efficient performance in all kinds of designed sequential circuits. Though the dual edge triggered flipflops provides better performance, the problems of clock skew and jitter can occurs. Hence the optimization of pulse triggered flipflop can be done by using pulse enhancement techniques. Apart from several low power consumption techniques, the pulse control technique is used to control the discharging in critical paths. The pulse enhancement scheme is performed by means of implementing the pass transistor logic based AND gate design and generating the narrow pulses to trigger the latch. Here, there are several flipflop designs under several techniques are analysed and compared with the pulse enhancement technique. The post layout simulation is performed in 90 nanometer technology leads to better performance in terms of area, delay and power.

Index Terms - Pulse triggered flipflop, 90 nanometer technology, Pass Transistor Logic, sequential circuits.